AF/ZEW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): Dunlop et al.
Case: 13-6
Serial No.: 09/716,977
Filing Date: November 20, 2000
Group: 2634
Examiner: Eva Y. Zheng

Title: Gated Clock Recovery Circuit

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Signature: Date: February 1, 2005

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith are the following documents relating to the above-identified patent application:

1. Appeal Brief (original and two copies); and
2. Copy of Notice of Appeal, filed on November 30, 2004, with copy of stamped return postcard indicating receipt of Notice by PTO on December 2, 2004.

There is an additional fee of $500 due in conjunction with this submission under 37 CFR §1.17(c). Please charge **Deposit Account No. 50-0762** the amount of $500, to cover this fee. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 50-0762** as required to correct the error. A duplicate copy of this letter and two copies of the Appeal Brief are enclosed.

Respectfully,

Date: February 1, 2005

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Patent Application

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APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby appeal the final rejection dated July 30, 2004, of claims 1 through 36 of the above-identified patent application.

REAL PARTY IN INTEREST

The present application is assigned to Lucent Technologies Inc., as evidenced by an assignment recorded on November 20, 2000 in the United States Patent and Trademark Office at Reel 011343, Frame 0645. The assignee, Lucent Technologies Inc., is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 1 through 36 are pending in the above-identified patent application. Claims 1-9, 11-21, 23-30, and 32-34 remain rejected under 35 U.S.C. §102(b) as being anticipated by Mittel et al. (United States Patent Number 5,610,558). The Examiner has already indicated that claims 10, 22, 31, 35, and 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

STATUS OF AMENDMENTS

Claim amendments to correct typographical errors (and, consequently, antecedent basis errors) were made in an Amendment After Final Rejection dated September 30, 2004, and have been entered for the purpose of appeal.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed to a gated clock recovery circuit that receives an input data stream and generates a frequency and phase aligned clock output. The gated clock recovery circuit substantially instantaneously adjusts the generated clock signal to phase changes in the incoming data stream. (Page 3, line 19, to page 4, line 16.) In addition, the gated clock recovery circuit generates the clock output signal using only transmitted non-predetermined data. The gated clock recovery circuit includes two PLL circuits. The first PLL (PLL1) adjusts to the frequency of the transmitter, and provides a bias voltage, CAP1, to the second PLL (PLL2) to indirectly initially tune the second PLL. The bias voltage, CAP1, is applied to the second PLL through a transmission gate (or switch) that is initially in a closed (short) position. Thus, the first PLL drives the bias voltage, CAP2, of the second PLL, to align the frequency with the transmitter, until received data opens the transmission gate. Thereafter, the bias voltage, CAP2, is removed and the second PLL can operate without being controlled by PLL1 so that the second PLL oscillates in phase with the received data. Simultaneously, the received data starts the oscillator in the second PLL so that the second oscillator is in phase with the received data. The second PLL then maintains this phase relationship between the second oscillator and the received data. (Page 4, line 17, to page 5, line 28.)

STATEMENT OF GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-9, 11-21, 23-30, and 32-34 are rejected under 35 U.S.C. §102(b) as being anticipated by Mittel et al.

ARGUMENT

Claim Rejections Under 35 USC §102(b) Over United States Patent Number 5,610,558

Independent Claims 1, 13, 25, 26 and 33

Independent claims 1, 13, 25, 26 and 33 are rejected under 35 U.S.C. §102(b) as being anticipated by Mittel et al. Regarding claim 1, the Examiner asserts that Mittel discloses wherein said second PLL circuit has a second mode wherein said second PLL has an initial frequency determined by said bias signal and whereby said second PLL substantially instantaneously adjusts said clock output signal to phase changes of data in an input data stream (reference signal 147). The Examiner further asserts that the phrases "initial" and "substantially instantaneously" form a contradiction for the second mode signal operation, and that it is confusing and unclear as to how the second PLL instantaneously adjusts to an unbiased signal while having a bias signal at the same time. In the Advisory Action, the Examiner further asserts that signal 214 is only set to bias during power up and that, when the power is down, the first PLL (202) will not use bias signal 214.

Contrary to the Examiner's assertion, the phrases "initial" and "substantially instantaneously" do not form a contradiction for the second mode signal operation. For example, consider that the time interval of the second mode of operation is labeled t. Immediately after the bias signal is removed and the second PLL enters the second mode of operation, it has an initial frequency associated with the start of time interval t. This initial frequency was established by the bias signal that was utilized in the first mode. Thus, although the second PLL is in the second mode of operation and the bias signal has been removed, the frequency of the second PLL has been established by the bias signal. Following entry into this second mode of operation, the second PLL substantially instantaneously adjusts the clock output signal to phase changes of data in an input data stream without utilization of the bias signal, potentially changing the frequency from its initial value. Thus, the second PLL can have an initial frequency established by the bias signal and can substantially instantaneously adjust the clock output signal

without utilizing the bias signal. Therefore, there is no contradiction between the phrases "initial" and "substantially instantaneously."

Applicants also note that Mittel teaches that

> the second filtered signal 321 is a current source signal that is combined with the tracking control signal 214. That is, the currents of these two signals are *added together* thereby creating a resultant current signal that coupled to the second oscillator 322.
> Col. 5, lines 22-26.

Tracking control signal 214 is generated by IDAC 330. IDAC 330 scales the oscillator control signal 212 generated by the master PLL 202 and *continuously* generates tracking control signal 214. Thus, the master PLL 202 continuously biases slave PLL 206. Mittel does not suggest or disclose that the master PLL 202 stops biasing the slave PLL 206. The independent claims require that the bias signal generated by a first PLL is not used to bias a second PLL in a second mode.

Thus, Mittel et al. does not disclose or suggest that the bias signal generated by a first PLL is not used to bias a second PLL in a second mode, as required by independent claims 1, 13, 25, 26, and 33.

It is clear from the present specification that the bias signal is not operative to influence the second PLL in the second mode. The gated clock recovery circuit of the present invention includes two PLL circuits. The first PLL (PLL1) adjusts to the frequency of the transmitter, and provides a bias voltage, CAP1, to the second PLL (PLL2) to indirectly initially tune the second PLL. The bias voltage, CAP1, is applied to the second PLL through a transmission gate (or switch) that is initially in a closed (short) position. Thus, the first PLL drives the bias voltage, CAP2, of the second PLL, to align the frequency with the transmitter, until received data opens the transmission gate. Thereafter, the bias voltage, CAP2, is *removed* and the second PLL can operate without being controlled by PLL1 so that the second PLL oscillates in phase with the received data. Thus, the present amendment is supported by the original specification.

Regarding the Examiner's assertion that signal 214 is only set to bias during power up, Applicants note that the term "power up" can be interpreted in two ways. If "power up" means "while the power is on," Applicants would agree with the Examiner's assertion. If, however, "power up" means "during the period when power is initially applied," Applicants

disagree since Applicants could find no disclosure or suggestion by Mittel that the bias signal is not utilized by the second PLL while it is on.

Regarding the Examiner's assertion that the first PLL (202) will not use bias signal 214 when the power is down, Applicants note that the independent claims require that the second PLL circuit generate a clock output signal in both modes of operation. The Examiner appears to define the second mode in Mittel (i.e., the mode when the first PLL is not biasing the second PLL) as the period of time when power is down. During power down, however, Mittel teaches that the second PLL is powered off in order to save power (col. 4, lines 1-4) and, thus, the second PLL cannot be generating a clock output signal, as required by the independent claims of the present invention.

Thus, Mittel et al. does not disclose or suggest that the bias signal generated by a first PLL is not used to bias a second PLL in a second mode, as required by independent claims 1, 13, 25, 26, and 33.

Claims 8, 9, 20 and 21

Claims 8/20 and 9/21 were rejected under 35 U.S.C. §102(b) as being anticipated by Mittel et al. Claims 8/20 require wherein said second mode is activated upon receipt of incoming data. Claims 9/21 require wherein receipt of incoming data substantially instantaneously starts said second PLL in phase alignment with said received incoming data. In particular, the Examiner asserts that Mittel et al. disclose the second mode is activated upon receipt of incoming data (col. 4, lines 1-11).

Applicants note that, in the text cited by the Examiner, Mittel discloses that "the slave PLL 206 is turned on and off periodically in order to save battery life. The turning on and off of the slave PLL 206 is controlled by the ON/OFF control signal 141 derived from the microprocessor control bus." Mittel later teaches that the mode of operation of the oscillator circuit 143 determines which clock signal is selected by the glitchless clock switch circuit 208, and that, "when the selective call receiver 100 is in standby mode (i.e., the power switch 128 has the receiver 124 powered down), the glitchless clock switch circuit 208 is programmed to select the first clock signal." (Col. 4, lines 13-19.) Thus, the modes taught by Mittel are determined by the power switch 128; the second mode is not activated upon receipt of incoming data.

Thus, Mittel et al. do not disclose or suggest wherein said second mode is activated upon receipt of incoming data, as required by claims 8 and 20, and do not disclose or

suggest wherein receipt of incoming data substantially instantaneously starts said second PLL in phase alignment with said received incoming data, as required by claims 9 and 21.

Claims 12 and 24

Claims 12 and 24 were rejected under 35 U.S.C. §102(b) as being anticipated by Mittel et al. Claims 12/24 require wherein said second PLL circuit generates said clock output signal using transmitted non-predetermined data. In particular, the Examiner asserts that Mittel et al. disclose the second PLL circuit generates said clock output signal using transmitted non-predetermined data (col. 2, lines 59-61).

Applicants note that, in the text cited by the Examiner, Mittel discloses:

> The system control circuit 137 is also coupled to the master-slave oscillator circuit 143, referred to herein as an oscillator circuit 143, providing the function of a phase-locked loop (PLL) for generating a microprocessor clock 144 coupled to the core circuitry of the system control circuit 137. The oscillator circuit 143 is also coupled to a time base reference oscillator 135 for generating a first reference signal 136.
> (Col. 2, lines 55-62.)

Mittel does not disclose or suggest, however, that the second PLL circuit generates said clock output signal using transmitted non-predetermined data.

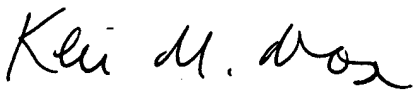
Thus, Mittel et al. do not disclose or suggest wherein said second PLL circuit generates said clock output signal using transmitted non-predetermined data, as required by claims 12 and 24.

Conclusion

The rejections of the cited claims under section §102 in view of Mittel et al. are therefore believed to be improper and should be withdrawn. The remaining rejected dependent claims are believed allowable for at least the reasons identified above with respect to the independent claims. The Examiner has already indicated that claims 10, 22, 31, 35, and 36 would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

The attention of the Examiner and the Appeal Board to this matter is appreciated.

Respectfully,



Date: February 1, 2005

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APPENDIX

1. A clock recovery circuit, comprising:

a first phase-locked loop (PLL) circuit for generating an oscillator signal having substantially the same frequency as a transmitter clock and for generating a bias signal; and

a second PLL circuit generating a clock output signal, wherein said second PLL circuit is controlled by said bias signal generated by said first PLL circuit in a first mode and wherein said second PLL circuit has a second mode wherein said second PLL has an initial frequency determined by said bias signal and whereby said second PLL substantially instantaneously adjusts said clock output signal to phase changes of data in an input data stream without utilizing said bias signal.

2. The clock recovery circuit of claim 1, wherein a transition between said first and second modes is controlled by a transmission gate.

3. The clock recovery circuit of claim 1, wherein a transition between said first and second modes is controlled by a switch.

4. The clock recovery circuit of claim 1, wherein a transition between said first and second modes is controlled by a device that selectively imposes a bias current from said first PLL to said second PLL.

5. The clock recovery circuit of claim 1, wherein a transition between said first and second modes is controlled by a device that selectively imposes a bias voltage from said first PLL to said second PLL.

6. The clock recovery circuit of claim 1, wherein said first PLL circuit is tuned to a local clock that operates at substantially the same frequency as a transmitter clock.

7. The clock recovery circuit of claim 1, further comprising an elastic storage circuit for generating a jitter-compensated clock and data output.

8. The clock recovery circuit of claim 1, wherein said second mode is activated upon receipt of incoming data.

9. The clock recovery circuit of claim 1, wherein receipt of incoming data substantially instantaneously starts said second PLL in phase alignment with said received incoming data.

10. The clock recovery circuit of claim 1, wherein said input data stream is a bit packet in asynchronous transfer mode format.

11. The clock recovery circuit of claim 1, wherein said first and second PLLs operate at different frequencies in accordance with one or more predefined ratios.

12. The clock recovery circuit of claim 1, wherein said second PLL circuit generates said clock output signal using transmitted non-predetermined data.

13. A method for recovering a clock signal from an incoming data stream, comprising:

tuning a first phase-locked loop (PLL) circuit to a local clock signal operating at substantially the same frequency as a transmitter clock, wherein said first PLL circuit produces a bias signal;

applying said bias signal to a second PLL circuit in a first mode, said second PLL circuit generating a clock output signal in said first mode having a frequency determined by said bias signal; and

removing said bias signal from said second PLL circuit in a second mode, wherein said second PLL circuit has an initial frequency in said second mode determined by said bias signal and whereby said second PLL substantially instantaneously adjusts said clock output signal to phase changes in said incoming data stream in said second mode.

14. The method of claim 13, wherein a transition between said first and second modes is controlled by a transmission gate.

15. The method of claim 13, wherein a transition between said first and second modes is controlled by a switch.

16. The method of claim 13, wherein a transition between said first and second modes is controlled by a device that imposes a bias current from said first PLL to said second PLL.

17. The method of claim 13, wherein a transition between said first and second modes is controlled by a device that imposes a bias voltage from said first PLL to said second PLL.

18. The method of claim 13, wherein said first PLL circuit is tuned to a local clock that operates at substantially the same frequency as a transmitter clock.

19. The method of claim 13, further comprising an elastic storage circuit for generating a jitter-compensated clock and data output.

20. The method of claim 13, wherein said second mode is activated upon receipt of incoming data.

21. The method of claim 13, wherein receipt of incoming data substantially instantaneously starts said second PLL in phase alignment with said received incoming data.

22. The method of claim 13, wherein said input data stream is a bit packet in asynchronous transfer mode format.

23. The clock recovery circuit of claim 13, wherein said first and second PLLs operate at different frequencies in accordance with one or more predefined ratios.

24. The clock recovery circuit of claim 13, wherein said second PLL circuit generates said clock output signal using transmitted non-predetermined data.

25. A clock recovery circuit, comprising:

a first phase-locked loop (PLL) circuit for generating an oscillator signal having substantially the same frequency as a transmitter clock and for generating a bias signal; and

a second PLL circuit generating a clock output signal, wherein said second PLL circuit has an initial frequency determined by said bias signal and wherein said second PLL circuit substantially instantaneously adjusts said clock output signal to phase changes of data of an input data stream when said input data stream is present without utilizing said bias signal.

26. A clock recovery circuit, comprising:

first means for generating a first oscillator signal having substantially the same frequency as a transmitter clock;

means for generating a bias signal;

second means for generating a clock output signal having an initial frequency determined by said bias signal and substantially instantaneously adjusting said clock signal output signal to phase changes of data in an input data stream without utilizing said bias signal; and

means for selectively imposing said bias signal from said first means to said second means.

27. The clock recovery circuit of claim 26, wherein said means for selectively imposing said bias signal is a transmission gate.

28. The clock recovery circuit of claim 26, wherein said means for selectively imposing said bias signal is a switch.

29. The clock recovery circuit of claim 26, wherein said means for selectively imposing said bias signal is a device that selectively imposes a bias current from said first means to said second means.

30. The clock recovery circuit of claim 26, wherein said means for selectively imposing said bias signal is a device that selectively imposes a bias voltage from said first means to said second means.

31. The clock recovery circuit of claim 26, wherein said means for selectively imposing said bias signal is a multiplexer.

32. The clock recovery circuit of claim 26, further comprising means for generating a jitter-compensated clock and data output.

33. A clock recovery circuit, comprising:

a first phase-locked loop (PLL) circuit for generating an oscillator signal having substantially the same frequency as a transmitter clock and for generating a bias signal;

a second PLL circuit generating a clock output signal in accordance with a control input;

a phase detector for generating an error signal indicating a difference in phase between an incoming reference signal and said clock output signal; and

a switch for selecting one of said bias signal and said incoming reference signal to generate said control input.

34. The clock recovery circuit of claim 33, wherein said clock output signal corresponds to phase changes of data of an input data stream in a second mode when said input data stream is present.

35. The clock recovery circuit of claim 33, wherein said multiplexer selects said bias signal in a first mode so that said second PLL has an initial frequency determined by said bias signal.

36. The clock recovery circuit of claim 33, wherein said multiplexer selects said error signal in a second mode so that said second PLL substantially instantaneously adjusts said clock output signal to phase changes of data in an input data stream.

Ryan, Mason & Lewis, LLP
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FAIRFIELD, CT 06824

Receipt in the USPTO is hereby acknowledged of:

Transmittal Letter – (Original & 1 copy)
Notice of Appeal - (Original & 1 copy)
Petition for Extension of Time (Original & 1 copy)

Case Name: Dunlop 13-6
Serial No.: 09/716,977

1150-454

November 30, 2004 KMM

1150-454

November 30, 2004 KMM

PTO/SB/31 (02-01)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

NOTICE OF APPEAL FROM THE EXAMINER TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Docket Number (Optional): Dunlop 13-6

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Assistant Commissioner for Patents, Washington D.C. 20231" on November 30, 2004.

Signature: Tina Maurice

Typed or printed name: Tina Maurice

In re Application of: Sayeed et al.

Application Number	Filed
09/716,977	November 20, 2000

For: Gated Clock Recovery Circuit

Group Art Unit	Examiner
2634	Eva Y. Zheng

Applicant hereby **appeals** to the Board of Patent Appeals and Interferences from the last decision of the examiner.

The fee for this Notice of Appeal is (37 CFR 1.17(b)) $340.00.

- ☐ Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee shown above is reduced by half, and the resulting fee is: $_____.
- ☐ A check in the amount of the fee is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Commissioner has already been authorized to charge fees in this application to a Deposit Account. I have enclosed a duplicate copy of this sheet.
- ☑ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 50-0762. I have enclosed a duplicate copy of this sheet.
- ☐ A petition for an extension of time under 37 CFR 1.136(a) (PTO/SB/22) is enclosed.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☑ attorney or agent of record.
- ☐ attorney or agent acting under 37 CFR 1.34(a). Registration number if acting under 37 CFR 1.34(a)._____.

Kevin M. Mason
Signature

Kevin M. Mason
Typed or printed name

November 30, 2004
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.